CLAIMS

What is Claimed is:

1. A method of forming an isolation region in a semiconductor substrate comprising the steps of:

a) annealing a liner oxide in a trench in the surface of said semiconductor substrate, and

b) backfilling said trench with a bulk oxide.

2. The method according to Claim 1 wherein said semiconductor substrate comprises silicon.

3. The method according to Claim 1 wherein said liner oxide comprises silicon dioxide.

4. The method according to Claim 1 wherein said bulk oxide of said step b) comprises silicon dioxide.

5. The method according to Claim 1 wherein said annealing step further denudes and getters at least one of said substrate and said liner oxide.

6. The method according to Claim 1 wherein said annealing step reduces stresses in said liner oxide.

7. The method according to Claim 1 wherein said annealing step reduces the number of dislocations in said semiconductor.

8. The method according to Claim 1 further comprising the step of etching a trench in the surface of said semiconductor substrate and wherein said step of etching is done using plasma etching said semiconductor substrate to form said trench.

9. The method according to Claim 1 wherein said step b) is done using chemical vapor deposition.

10. The method according to Claim 1 wherein said annealing step further reduces the leakage between active regions in said semiconductor substrate.

11. A process for reducing leakage in forming an integrated circuit, structure comprising the steps of;

a) annealing a liner oxide layer in a shallow trench within a semiconductor substrate under conditions sufficient to reduce the rate of dislocations within said integrated circuit; and

b) chemical vapor depositing an oxide in said shallow trench.

12. A process as described in Claim 11 further comprising the steps of:

using a plasma etching process to form said shallow trench within said semiconductor substrate; and

growing a liner oxide layer over the surfaces of said shallow trench.

13. A process as described in Claim 11 wherein said annealing step is performed to also increase the density of said liner oxide.

14. A process as described in Claim 11 wherein said substrate further comprises a layer containing polysilicon over said shallow trench, and said method further comprises the step of performing a polysilicon etch over said shallow trench.

15. A process as described in Claim 11 wherein said step a) is performed also to achieve gettering and denuding.

16. A process as described in Claim 11 wherein said shallow trench is no greater than approximately 0.3 microns wide.

17. The process according to Claim 11 wherein said semiconductor is silicon.

18. The process according to Claim 11 wherein said liner oxide is silicon dioxide.

19. The process according to Claim 11 wherein said oxide of said step d) is silicon dioxide.

20. The process according to Claim 11 wherein said annealing step reduces relieves stresses in said liner oxide.

21. The process according to Claim 11 wherein said annealing step allows the width of the trench to be smaller than that realized without said annealing step.

22. The process according to Claim 11 wherein said annealing further reduces the leakage between active regions in said semiconductor.

23. A process for forming the isolation regions in a semiconductor substrate comprising the steps of:

a) etching a trench in the surface of said semiconductor substrate, said trench having corners therein;

b) growing a liner oxide in said trench;

c) annealing said liner oxide to reduce stresses at said corners; and

d) backfilling said trench with a bulk oxide.

24. The process according to Claim 23 wherein said linear oxide is increased in density as a result of said steps c) and d).

25. The process according to Claim 23 wherein said step c) reduces the number of dislocations formed in said substrate.

26. A process for growing and annealing liner oxide (LINOX) in a trench formed on the surface of a semiconductor comprising;

a) growing said liner oxide in said trench at a first temperature, and

b) annealing said liner oxide at a second temperature higher than the first temperature elevated above that used in said step a) sufficient to reduce relieve stresses in said liner oxide.

27. The process according to Claim 27 wherein denuding and gettering are achieved in said semiconductor during annealing said liner oxide.

28. The process according to Claim 27 wherein the leakage between active regions in said semiconductor is improved.